material P1 covers part of the third doped region of type one D_13. Therefore, in FIG. 8(*a*), no silicide is provided on at least part of the well of type one W_1 adjacent to the third doped region of type one D_13, and at least part of the third doped region of type one D_13 adjacent to the well of type one W_1. The third doped region of type one D_13 is coupled to an operational voltage VDD and the third doped region of type two D_23 is coupled to another operational voltage VSS in this embodiment.

For the embodiment shown in FIG. 3, the semiconductor device **300** comprises similar structure for which of the semiconductor device **200**. One of the differences is the first type is changed from the N type to the P type, and the second type is changed from the P type to the N type in FIG. 3. Additionally, the operational voltages VDD, VSS are swapped. Furthermore, current path CP is inversed, thus it is from the VDD provided to the first doped region of type one D_11 to IO. Moreover, the voltages TP, TN are swapped. FIG. 8(*b*) illustrates the situation that the semiconductor device **300** comprises silicide SI. Other structures and operations for the semiconductor device **300** can be clearly understood based on the description for FIG. 2, thus it is omitted for brevity here.

The substrate S in the semiconductor device **400** in FIG. 4 also comprises the well of type one W_1, the first doped region of type two D_21, the well of type two W_2, the first doped region of type one D_11, the third doped region of type one D_31 and the second doped region of type one D_32. However, the semiconductor device **400** comprises only the second doped region of type two D_22 rather than the first conductive material CM_1, the second conductive material CM_2, the second doped region of type one D21 and the second doped region of type two D_22 in FIG. 2. In the semiconductor device **400**, the second doped region of type two D_22 does not touch the first doped region of type one D_11 and the first doped region of type two D_21. Additionally, the second doped region of type two D_22 in FIG. 4 receives a voltage PTR to assist transmitting the current.

During the manufacturing of the semiconductor device **400**, the semiconductor device **400** also comprises protecting material P_1. Besides, the semiconductor device **400** further comprises the protecting material P_2 and the protecting material P_3. The protecting material P_2 is provided on at least part of the first doped region of type two D_21, at least part of the second doped region of type two D_22, and at least part of the well of type one W_1 between the first doped region of type two D_21 and the second doped region of type two D_22. The protecting material P_3 is provided on at least part of the first doped region of type one D_11, at least part of the second doped region of type two D_22, and at least part of the well of type two between the first doped region of type one D_11 and the second doped region of type two D_22. Therefore, the silicide SI is not provided at the locations for the protecting materials P_1, P_2 and P_3, as shown in FIG. 9(*a*).

The semiconductor device **500** in FIG. 5 comprises similar structure for which of the semiconductor device **400**. One of the differences is the first type is changed from the N type to the P type, and the second type is changed from the P type to the N type in FIG. 5. Additionally, the operational voltages VDD, VSS are swapped. Furthermore, current path CP is inversed, thus it is from the VDD provided to the first doped region of type one D_11 to 10. FIG. 9 (*b*) illustrates the situation that the semiconductor device **500** comprises silicide SI. Other structures and operations for the semiconductor device **500** can be clearly understood based on the description for FIG. 4, thus it is omitted for brevity here.

FIG. 6 is a schematic diagram illustrating a semiconductor device **600** according to another embodiment of the present application. The only difference between the embodiments in FIG. 4 and FIG. 6 is that the second doped region of type two D_22 does not touch the first doped region of type one D_11 in FIG. 4, but the second doped region of type two D_22 touches (or overlaps) the first doped region of type one D_11 in FIG. 6. Therefore, the protecting material P_3 in FIG. 6 is provided on at least part of the first doped region of type one D_11, and at least part of the second doped region of type two D_22. The silicide SI is not provided at the locations for the protecting materials P_1, P_2 and P_3 of FIG. 6, as shown in FIG. 10 (*a*).

The semiconductor device **700** in FIG. 7 comprises similar structure for which of the semiconductor device **600**. One of the differences is the first type is changed from the N type to the P type, and the second type is changed from the P type to the N type in FIG. 6. Additionally, the operational voltages VDD, VSS are swapped. Furthermore, current path CP is inversed, thus it is from the VDD provided to the first doped region of type one D_11 to 10. FIG. 10 (*b*) illustrates the situation that the semiconductor device **700** comprises silicide. Other structures and operations for the semiconductor device **700** can be clearly understood based on the description for FIG. 6, thus it is omitted for brevity here.

The voltages TP, TN in FIG. 2 and FIG. 3, and the voltages PTR,NTR in FIG. 4-FIG. 7, are applied for assisting the transmitting of the currents, as above-mentioned. The values thereof depend on the types of channels for the current path. In the embodiments of FIG. 2-FIG. 7, the voltage TN is higher than the voltage TP, and the voltage PTR is higher than the voltage NTR. FIG. 11 is a circuit diagram illustrating a voltage providing circuit **1100** for providing voltages to the semiconductor devices disclosed in the present application, according to one embodiment of the present application. As shown in FIG. 11, the voltage providing circuit **1100** is a RC inverter. A higher voltage, such as TN or PTR can be derived from the output of the voltage providing circuit **1100**, and a lower voltage, such as TP or NTR, can be derived from the input of the voltage providing circuit **1100**. Please note the circuit for providing the voltages TP, TN, PTR, NTR are not limited to the circuit structure shown in FIG. 11.

In view of the above-mentioned embodiments, no STI is provided between P doped region and the N doped region, thus the current path is shorter and the discharging time for the semiconductor device is reduced. Also, voltage assisting the current transmitting can be provided to the semiconductor device. By this way, the circuit need to be protected can be well protected if the disclosed semiconductor device is applied as an ESD device.

Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A semiconductor device, comprising:

a substrate, comprising:

a well of type one;

a first doped region of type two, provided in the well of type one;

a well of type two, adjacent to the well of type one;